(e) disposing an integrated circuit die on the first surface of the substrate.

20. (original) The method, as set forth in claim 19, wherein act (a) comprises providing a board-on-chip substrate.

21. (original) The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method.

22. (original) The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to ultraviolet energy.

23. (original) The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to downstream plasma etching.

24. (original) The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to reactive ion etching.

25. (original) The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to wet chemical etching.

26. (original) The method, as set forth in claim 21, wherein act (c) comprises exposing the second portion of the solder resist to radiation etching.

27. (original) The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method to raise the surface tension to at least 31 dynes/cm.

28. (original) The method, as set forth in claim 19, wherein act (c) comprises exposing the second portion of the solder resist to an activation method to raise the surface tension to at least 54 dynes/cm.

29. (original) The method, as set forth in claim 19, wherein act (c) comprises disposing a memory device onto the first surface of the substrate.

30. (new) The method, as set forth in claim 19, wherein the acts (a), (b), and (c) are performed in the order recited.